Appeal No. 2015-1072

United States Court of Appeals for the Federal Circuit

HARMONIC INC.,
Petitioner-Appellant,

v.

AVID TECHNOLOGY, INC.,
Patent Owner-Appellee,

Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board No. IPR2013-00252

OPENING BRIEF OF PATENT OWNER-APPELLEE

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CERTIFICATE OF INTEREST

Pursuant to Federal Circuit Rule 47.4, undersigned counsel for Appellee Avid Technology, Inc., certifies the following:

1. The full name of every party or amicus represented by me is: Avid Technology, Inc.

2. The names of the real parties in interest, if different from the parties named above, are: Not applicable.

3. The names of all parent corporations and any publicly held companies that own 10% or more of the stock of the party represented by me are: Blum Capital Partners, L.P.; Wells Fargo & Co.

4. The names of all law firms and the partners and associates that appeared for Appellee in the trial court or agency or are expected to appear in this court are:

JONES DAY: Gregory A. Castanias; David B. Cochran; Joseph M. Sauer; Matthew W. Johnson; Henry Leon (Lon) Outland III.

Dated: April 27, 2015

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Parties

Avid	Plaintiff-Appellant Avid Technology, Inc.
Harmonic	Defendant-Appellee Harmonic, Inc.

Cites

A__	Joint Appendix at page(s) __
A__:__	Joint Appendix at page __: line __
HBr. __	Harmonic Opening Brief at page(s) __

Terms

’291 Patent	U.S. Patent No. 5,495,291
Board or PTAB	Patent Trial and Appeal Board
IPR	*Inter Partes* Review
USPTO	United States Patent and Trademark Office

STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, counsel for Appellant Avid Technology, Inc., provides as follows:

1. There has been no previous appeal in this case.

2. Counsel is aware of two cases pending before this Court that may directly affect part of this Court's decision in this appeal. *Shaw Industries Group, Inc. v. Automated Creel Systems, Inc.*, Nos. 2015-1116, -1119 and *Schott Gemtron Corp. v. SSW Holding Co. Inc.*, No. 2015-1073 relate to the PTAB's authority to deem grounds of unpatentability redundant.

JURISDICTIONAL STATEMENT

The Patent Trial and Appeal Board had jurisdiction over this *Inter Partes* Review proceeding pursuant to 35 U.S.C. § 6. After the conclusion of the IPR trial, the Board entered a Final Written Decision on July 10, 2014, finding that Petitioner Harmonic had not proven that certain claims of the '291 Patent were unpatentable. On September 11, 2014, Harmonic filed a Notice of Appeal. This Court has jurisdiction over this appeal pursuant to 28 U.S.C. § 1295(a)(4)(A).

COUNTER-STATEMENT OF THE ISSUES

1. Whether the Board acted within its discretion by declining to consider a new argument first raised by Harmonic in its Reply before the Board, and not presented in Harmonic's Petition.

2. Whether the Board's refusal to consider Harmonic's belated argument was harmless, in view of the fact that the Board nonetheless considered Harmonic's new argument and correctly found that the cited reference (Haskell) failed to teach or suggest the presence of a controller that meets the missing limitation of claim 11—providing a second set of video data at a second rate "a predetermined period of time" after the first set of video data starts to be received.

PRELIMINARY STATEMENT

This case involves a patent owned by Avid that claims a video processing system for playing multiple video streams, one after the other, with no appreciable delay between the video stream playback. Such delays previously occurred when systems would transition from playing one video stream to the next. The inventions claimed in the Avid patent enable video to continue playing without interruption during the transition between video streams.

Harmonic filed a Petition for *Inter Partes* Review with the Board, requesting review of claims 1-20 of the '291 Patent. The Board declined to review claims 17-20, but instituted a trial to review the patentability of claims 1-16. The trial was instituted based on the combination of two references: Haskell and Rossmere. The Board ultimately determined Harmonic failed to prove that claims 11-16 were unpatentable. Harmonic now appeals that decision.[1]

In the course of the IPR proceeding, the Board rightly refused to consider new evidence that Harmonic first introduced in its Reply, to which, by rule, Avid was not permitted to respond. Once an IPR is instituted, based on the challenger's Petition, the patent owner has only one briefing opportunity to support the patentability of the claims under review—the Patent Owner Response. Then, the

[1] The Board did hold that claims 1-10 were unpatentable under 35 U.S.C. § 103(a). (A27.) Avid has not appealed that aspect of the decision.

challenger, in its Petitioner Reply, has the last word on paper to the Board. In its Petition and supporting Declaration, Harmonic mentioned claim 11 of the '291 patent in only the most cursory fashion. After Avid identified, in its Patent Owner Response, the severe deficiencies in Harmonic's treatment of claim 11, Harmonic cited to entirely new evidence its Petitioner Reply to attempt to overcome these deficiencies. Harmonic's sandbagging was highly prejudicial to Avid, because Avid had no opportunity to respond.

In its Final Written Decision, the Board rightly recognized Harmonic's improper new evidence and argument, ruling that "Petitioner's improper argument raised for the first time in the Reply will not be considered, because it is not accompanied by a showing of good cause explaining why it could not have been presented in the Petition." (A26.) The Board determined that the cursory evidence presented by Harmonic in its Petition was insufficient. Thus, claims 11-16 were deemed patentable.

Harmonic's arguments on appeal challenging the Board's determination do not hold water. *First*, Harmonic's contention that its Reply brief did not improperly present new evidence is wrong because, among other things, Harmonic cited to a never-before-discussed feature of the Haskell reference for the first time in the Reply. This left Avid without any recourse to respond.

Second, Harmonic's argument that the Board's determination of unpatentability for independent claims 1 and 9 also means that dependent claims 11-16 are unpatentable is unsupportable. Claim 11 (and the other independent claims) are necessarily narrower than independent claim 9 from which they depend. Harmonic's four-sentence argument about claim 11 in its Petition failed to account for a critical limitation of claim 11 of providing a second set of video data at a second rate "a predetermined period of time" after the first set of video data starts to be received. Harmonic's Reply failed to remedy the deficiency—indeed, even the new, improperly-cited evidence failed to disclose the critical limitation.

The Board's judgment sustaining claims 11-16 of the '291 Patent as patentable should be affirmed.

STATEMENT OF THE CASE

A. Overview of the '291 Patent

The '291 Patent is directed to a video processing system that enables multiple video streams to be played, one after the other, with no appreciable delay between videos. (*See, e.g.*, A34 at 2:21-43.) The inventors of the '291 Patent recognized that when two video programs are played consecutively using prior art systems, the delay caused by buffering and data processing often causes blank frames to be generated between video programs. (*Id.*) The '291 Patent addresses this problem by beginning to process and buffer a second video stream while a first

video data stream is still being played. The second video data stream may then begin playback as soon as the first video stream ends. (A34-35 at 2:47-3:5.)

An exemplary embodiment described in the '291 Patent is illustrated in Figure 3, reproduced below.

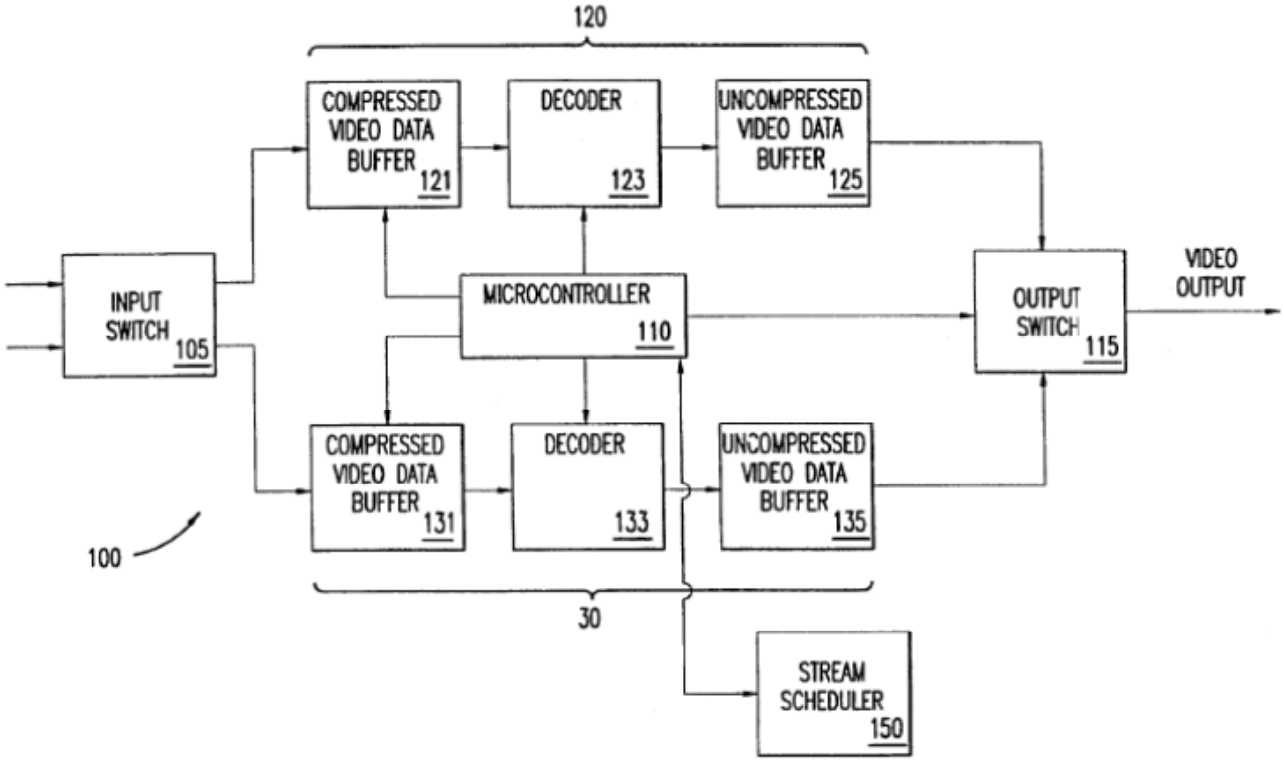


FIG.3

The system of Figure 3 provides a continuous video output from a plurality of video inputs by controlling the flow rate of the video inputs into the video data buffers and by controlling an output switch 115 to provide continuous output video data. The system includes an input switch 105 that receives two separate video streams. Under control of microcontroller 110, the input switch 105 regulates the

flow rate of the video streams into two parallel decompression circuits 120, 130 (decompression circuit 130 is mistakenly labeled "30" in Figure 3).

The parallel decompression circuits 120, 130 and the flow rate are controlled so that decompressed video data from the second video stream is available for output when the first video stream is complete. Specifically, the first decompression circuit 120 receives video data at a first, high rate, and the second decompression circuit 130 receives video data at a second, lesser rate. (A35 at 4:37-5:10.) As compressed video data is received by the first decompression circuit 120, it is buffered by compressed video data buffer 121, decoded by decoder 123, buffered again by uncompressed video data buffer 125, and output by output switch 115. (*Id.* at 4:53-63.)

When the first video stream is nearly finished, microcontroller 110 instructs input switch 105 to cause the second video stream to begin flowing into the second decompression circuit 130 at the second, lower rate. (*Id.* 4:64-5:10.) In this way, once the first video program flowing into the first decompression circuit 120 ends, the second decompression circuit 130 has multiple frames of video data already decompressed and waiting for immediate display or output. (A36 at 5:11-30.) Microcontroller 110 instructs the output switch 115 to switch the output to the second decompression circuit 130 as the output from the first decompression

circuit 120 ends, thus providing a continuous generation of decompressed video data. (*Id.)*

Claim 9, from which claim 11 depends, recites:

> 9. A video decompression system comprising:
>
> a first switch coupled to at least two video data input lines, the first switch controlling the direction and rate of video data flow from the video data input lines;
>
> at least two video data decompression arrays coupled to the first switch, the video data decompression arrays storing compressed video data, decompressing the stored compressed video data, and storing the decompressed video data;
>
> a second switch coupled to the video data decompression arrays and to an output bus, the second switch directing output from the at least two video data decompression arrays to the output bus; and
>
> a controller coupled to the first switch, the video data decompression arrays, and to the second switch for controlling the flow of video data through the system.

(A37 at 7:4-20.) This claim recites, among other elements, "a first switch coupled to at least two video data input lines, the first switch controlling the direction and rate of video data flow from the video data input lines," which reads on the input switch 105 described in the specification. (*See* A35-36 at 4:38-5:30.)

The claim also recites "a controller coupled to the first switch, the video data decompression arrays, and to the second switch for controlling the flow of video data through the system." This claim feature reads on microcontroller 110. Claim 11 elaborates on the functionality of the controller and the first switch stating:

> 11. The system of claim 9 wherein the controller commands the first switch to provide video data to the first video data decompression array at a first rate and to provide video data to the remaining video data decompression arrays at a second rate *a predefined period of time after the first video data array begins receiving the video data* at the first rate.

(A37 at 7:27-32 (emphasis added).) This limitation requires that the controller command the first switch to provide video data to the remaining data decompression arrays (*e.g.*, second decompression circuit 130) "a predefined period of time after the first video data array begins receiving the video data," where that timing is predefined relative to the controller.

B. Harmonic's Cited References

Harmonic's Petition requested a trial based on seven different grounds of unpatentability. (A45.) The Board denied all of those grounds except one. (A75.) The Board instituted trial only to determine whether claims 1-16 were unpatentable based on the combination of Haskell and Rossmere. (*Id*.) Because Harmonic has never alleged that Rossmere teaches the critical limitation of claim 11, the discussion that follows is limited to Haskell.

Haskell relates to avoiding encoder and decoder buffer overflow and underflow when transmitting images over a variable bit-rate channel. (A289 at 1:6-9.) Haskell notes that "[o]verflow of the encoder buffer causes data to be lost," while "[u]nderflow of the buffer results in inefficient use of the transmission channel bandwidth." (*Id*. at 1:29-32.)

Haskell proposes to overcome the "problems of buffer overflow and underflow encountered when employing actually variable or effectively variable bit-rate channels for communicating encoded video images . . . by jointly controlling the number of bits employed to encode each video frame and the transmission bit-rate of the variable bit-rate channel as experienced by the encoder." (*Id*. at 2:5-13.) By controlling those two variables, (*i.e.*, (1) the number of bits employed to encode each video frame, and (2) the transmission bit-rate) on the encoder side of the transmission channel, Haskell purports to prevent buffer overflows and underflows on both the encoder and decoder sides of the apparatus.

The Petition's proposed ground of rejection of claims 9 and 11 relied on a combination of the Figure 2 and Figure 3 embodiments of Haskell, depicted below:

FIG. 2

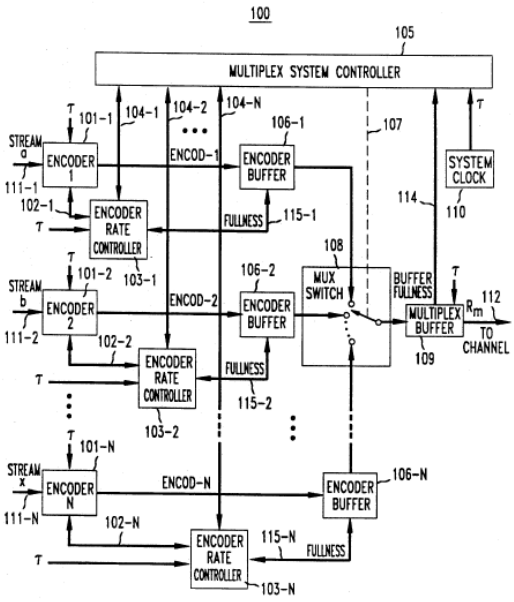


FIG. 3

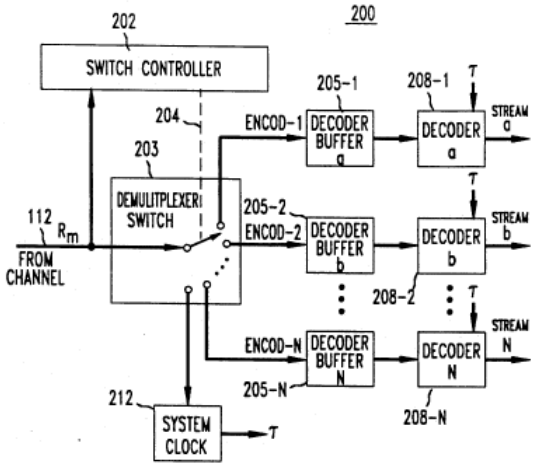


Figure 2 shows an encoder system 100, and Figure 3 depicts a decoder system 200. (A289 at 2:56-61.) These systems are connected together by a channel 112, which could be any form of communication medium. The encoding system 100 includes a multiplex controller 105, encoders 101, encoder buffers 106, a multiplexer switch 108, and a multiplexer buffer 109. Unencoded bit-streams 111-1 through 111-N are encoded by the encoders 101 and multiplexed at 108 into a single bit-stream 112 as commanded by the system controller 105 for transmission. (A294 at 11:67-12:19.)

While the encoder system 100 transmits data in such a way to keep the decoder buffers from underflowing or overflowing, it does not transmit data as a continuous stream. Instead, packets (each containing one access unit) produced by the encoders 101 are gathered temporarily in the multiplexer buffer 109 and then sent as "packs" of packets according to "predetermined system timing" (A295 at 13:7-20.)[2] Periodically, all of the packets to be sent by the encoder 100 are positioned in multiplexer buffer 109 and transmitted as a group. (*See* A295 at 14:12-31 (referencing Figure 5, where access units from streams a, b, c, and d are transmitted, but no access unit from e is transmitted because the encoder has not

[2] Harmonic did not cite to this feature of Haskell in any manner in its Petition. The predetermined system timing feature is nevertheless explained here to provide context for later discussions.

yet decided to place an access unit from e into the multiplexer buffer).) The encoder 100 decides which packets are to be included in each periodic transmission and how those packets are encoded. (*Id.* at 14:12-14.)

On the decoder side, demultiplexer switch 203 receives compressed data streams from the encoder over channel 112. (A295 at 13:35-54.) The switch controller 202 identifies the data stream from which the data is being received and commands the demultiplexer switch 203 to route that data to a corresponding decoder path 205, 208. (A295 at 13:35-41.) The decoder paths include decoder buffers 205 for temporary storage of incoming data. (*Id*. at 13:39-48.) The decoder buffers 205 are coupled to decoders 208 that decode data received from the buffers 205 and output decompressed data streams. (*Id*.)

C. The PTAB Proceeding

1. Harmonic's Petition

Harmonic's Petition for *Inter Partes* Review proposed seven grounds of unpatentability of the claims of the '291 Patent. The Petition included a declaration by Dr. Kenneth Zeger. (A102-77.) With respect to the alleged obviousness of claims 9 and 11 based on Haskell and Rossmere, the declaration of Dr. Zeger repeats the arguments set forth in the Petition nearly *verbatim*. (*See* A89-91, A161-62.) The Declaration includes no additional evidence or reasoning to back up the legal arguments set forth in the Petition. Because the Declaration

offers no additional substance, the remainder of this discussion references only the Petition.

In arguing that claim 9 is obvious, Harmonic cited to Figures 2 and 3 of Haskell as disclosing the first switch, the decompression arrays, and the controller, and cited to Rossmere as disclosing the second switch. (A89-90.) Harmonic argued that the encoder functionality in Haskell discloses the data flow control aspects of the independent claims. (A89 at 90 ("Encoder 100 controls the flow of data through the decoder unit.").)[3]

Harmonic devoted two full pages to the alleged obviousness of independent claim 9, but devoted only five sentences to claim 11, the first of which merely repeated the claim language:

> **Claim 11**: Haskell discloses that the controller is capable of commanding the first switch to provide video data to the first video data decompression array at a first rate and to provide video data to the remaining video data decompression arrays at a second rate a predefined period of time after the first video data array begins receiving the video data at the first rate. For example, Haskell teaches the ability to individually control the incoming bitrate for each decoder. *See* Ex. 1008 at 2:28-32; 2:41-44. Haskell also discloses the ability to switch packets from disparate streams between a plurality of decoder units, one for each given stream. *See*, *e.g.*, demux switch 203

[3] Avid disagreed that consideration of encoder-side functionality was appropriate in considering the video decompression system of claims 9 and 11. (*See*, *e.g.*, A511-12.) But the Board found such citations by Harmonic acceptable in the Final Written Decision. (A18-19.) Avid does not further contest this point.

> of Haskell (Ex. 1008) at Fig. 3, 13:35-54. Thus, all claim limitations are met. *See, e.g.*, Ex. 1002 ¶282.

(A91.) These sentences address bit-rate control, citing to 2:28-32 and 2:41-44 of Haskell. (*Id*., citing A289:2:28-32 and A289:2:41-44.) They further address switching packets from disparate streams among the decoder units, citing to demux switch 203 and 13:35-54 of Haskell (A282 Fig. 3; A295:13:35-54).

Harmonic's Petition nonetheless failed to address a critical limitation of claim 11—the one requiring that the controller "provide video data to the remaining video data decompression arrays at a second rate *a predefined period of time after the first video data array begins receiving the video data*." (A37 at 7:29 32 (emphasis added).)

2. **The Board's Institution Decision**

On September 25, 2013, the Board instituted review of claims 1-16, based only on the Haskell and Rossmere obviousness ground. (A456-69.) The Board declined to institute review as to the remaining proposed grounds for claims 1-16 on the basis that they were redundant. (A474.) The Board did not institute trial on any ground related to claims 17-20. (A469-74.)

3. **Avid's Response**

Avid filed its Patent Owner Response on December 9, 2013. With regard to independent claims 1 and 9, Avid argued that consideration of Haskell's encoder

side functionality was not appropriate because the '291 patent claimed a "video decompression system."

For claim 11, Avid made two arguments. First, Avid argued that encoder side functionality was not relevant to a decompression system. Avid also argued that Harmonic failed to identify in the prior art the "predefined period of time feature" of claim 11:

> [T]he citations to column 2 and the subsequent citation to the demultiplexer switch 203 of FIG. 3 at column 13 do not at all account for the "predetermined period of time" language of claim 11. The Haskell demultiplexer switch 203 connects the multiplex data stream 112 to the proper decoder buffer 205 as packets arrive. The demultiplexer switch 203 has no control over when packets arrive, as that is encoder functionality in Haskell. (*Id*., 13:7-20.) Thus, there is no "provid[ing] video data to the remaining video decompression arrays… ***a predefined period of time*** after the first video data array begins receiving the video data at the first rate," as required in claim 11.

(A527 (emphasis in original).) Avid argued that Harmonic's citations to Haskell (A289) at 2:28-32 and 2:41-44 were only relevant to bit-rate control. Avid also pointed out that decoder demultiplexer switch 203 could not provide the claimed controller's data routing function because all data flow control was encoder side in Haskell, as described at 13:7-20 (A295). Because Harmonic wholly ignored claim 11's critical "predefined period of time" feature, Avid argued that claim 11 could not be found unpatentable.

4. **Harmonic's Reply**

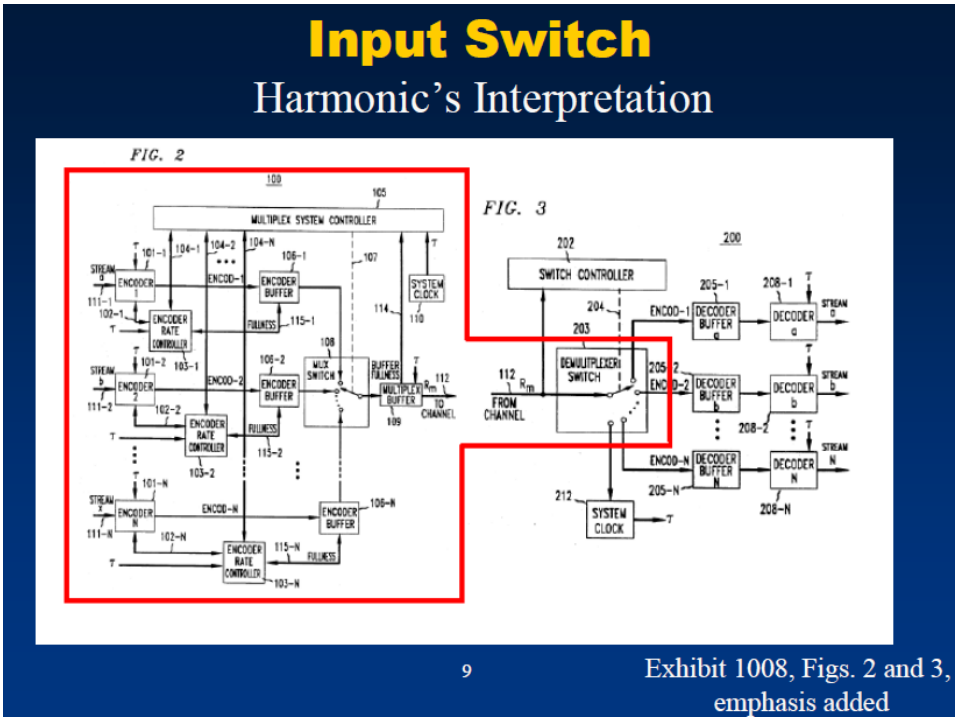
Harmonic filed its Reply on February 25, 2013. (A532-39.) Harmonic addressed Avid's first claim 11 argument, responding that the encoder side functionality should not be ignored. (A546-47.) But in responding to Avid's second argument—that Harmonic ignored the "predefined period of time feature" in claim 11 and thus failed in its proofs—Harmonic attempted to rely on a new feature of Haskell that it had never mentioned in its Petition:

> There is also no basis for Avid's contention that Haskell does not suggest "provid[ing] video data to the remaining video decompression arrays . . . a predefined period of time after the first video data array begins receiving the video data at the first rate." *Haskell explicitly discloses the use of predetermined system timing with regard to providing video data to decode buffers* (205-1, 205-2, 205- N). *See* Ex. 1008 at 13:7-54.

(A547 (emphasis added).) This was the first time in the proceeding that any party mentioned Haskell's periodic transmission of packs of packets based on predetermined system timing to be relevant to any of the claims of the '291 Patent.

5. **Oral Argument**

At oral argument, Avid illustrated the hardware in Figures 2 and 3 of Haskell that Harmonic alleged disclosed the claimed input switch.



Avid responded that Harmonic's argument was unreasonable because the preamble of claim 9 limited the claim to a decompression system, and what Harmonic relied on was the compression hardware of Haskell. (A685 at 3-12; A576.)

6. The Board's Final Written Decision

The Board's Final Written Decision started with claim construction. (A7-12.) Of note, the Board construed "a predefined period of time," as recited in claim 11, to mean "a prior defined period of time." (A10.)

As to unpatentability, the Board determined that claims 1-10 were unpatentable based on Haskell and Rossmere. (A17-25.) The Board agreed that Avid's "arguments are predicated incorrectly on the demultiplexer switch 203 alone as teaching or suggesting the claimed input switch, and disregard the claim

construction of 'switch' as including 'a device or assembly for routing or selecting a data stream.'" (A18.) The Board found that the demultiplexer switch 203 of decoder 200 together with multiplexer switch 108 of encoder 100 taught the claimed input switch and that encoder 100 controls the flow of data through decoder 200. (A18.)

With respect to claims 11-16, however, the Board agreed with Avid that Harmonic "did not account for the 'predefined period of time' language of claim 11." (A26.) The Board refused to consider Harmonic's late reference to the "predetermined system timing" feature of Haskell, stating:

> In the Reply, Petitioner asserts *for the first time* that Haskell teaches or suggests "provid[ing] video data to the remaining video decompression arrays . . . a predefined period of time after the first video data array begins receiving the video data at the first rate," because Haskell discloses the use of a predetermined system timing with regard to providing video data to decoder buffers (205-1, 205-2, 205-N). Pet. Reply 13 (citing Ex. 1008, col. 13, ll. 7-54). Petitioner's arguments in the Reply are improper because they are not responsive to arguments raised in the Patent Owner Response. *See* 37 C.F.R. § 42.23. Patent Owner's Response does not direct attention to Haskell's disclosure of using a predetermined system timing for providing video data to the decoder buffers. *See* PO Resp. 33-35. Petitioner's improper argument raised for the first time in the Reply will not be considered, because it is *not accompanied by a showing of good cause explaining why it could not have been presented in the Petition*.

(*Id*. (emphasis added).)

Although the Board officially refused to consider the "predetermined system timing" feature of Haskell in assessing the patentability of claim 11, the Board noted that even if that feature was considered, it would not be sufficient:

> In any event, even if Petitioner's arguments were to be considered, Petitioner does not explain sufficiently how Haskell's use of predetermined system timing for providing video data to decoder buffers (205-1, 205-2, 205-N), teaches or suggests a controller that commands the first switch to provide video data to the remaining video decompression arrays at a second rate a predefined period of time (*i.e.*, a prior defined period of time) after the first video data array begins receiving the video data at the first rate.

(A26-27.)

Based on these findings, the Board concluded that Harmonic had not shown that claims 11-16 were unpatentable. (A26-27.)

SUMMARY OF THE ARGUMENT

The Board's judgment that claims 11-16 are patentable should be upheld for at least the following reasons.

First, Harmonic failed to address all of the limitations of claims 11-16 in its Petition, and then attempted to present an improper new argument in its Reply. Such late arguments are appropriately rejected because they are highly prejudicial to patent owners, and could have been avoided by petitioners. Harmonic's Petition cited to four pieces of evidence in making a case for the unpatentability of claim 11.

(A91.)[4] None of these four citations related to Haskell's "predetermined system timing feature." In response, Avid pointed out that Harmonic completely ignored the critical "predefined period of time" limitation of claim 11, explaining that the demultiplexer switch is on the decoder side and thus "has no control over when packets arrive." (A527.) Neither Harmonic's Petition nor Avid's Response ever mentioned a "predetermined system timing" feature of Haskell. Thus, the Board properly excluded Harmonic's citation of new evidence in its Reply. (A26.)

Second, Harmonic's protest about the Board excluding its improper argument is ultimately irrelevant, because the Board also found Harmonic's new arguments substantively wanting. The Board expressly stated that, "[i]n any event, even if Petitioner's arguments were to be considered, Petitioner does not explain sufficiently how Haskell's use of predetermined system timing for providing video data to decoder buffers (205-1, 2052, 205-N), teaches or suggests the claimed feature." (A26-27.) Thus, even though the Board found that Harmonic had waived its argument by failing to properly present it in the Petition, the Board ultimately did consider Harmonic's new evidence and found it unpersuasive despite its procedural defects. On this latter point, Harmonic has no response.

[4] Harmonic cited to: (1) Haskell at 2:28-32; (2) Haskell at 2:41-44; (3) Demux switch 2003 of Haskell; and (4) Haskell at 13:35-54.

Further, Harmonic no longer maintains that the Haskell "predetermined system timing" feature renders claim 11 unpatentable. Indeed, Harmonic seeks to distance itself from the citation to that feature, saying it is unnecessary for a finding of unpatentability (HBr. 29-31), and does not even refer to that feature in arguing that the Board erred in its obviousness determination (HBr. 31-39). Nowhere in its brief does Harmonic even bother to explain how the Haskell "predetermined system timing" feature works.

Third, the Board correctly determined that claim 11 was not unpatentable based on the case that was actually presented by Harmonic. Harmonic tries to muddle the issues, arguing that because it was successful in challenging independent claim 9, it must also be successful in challenging claim 11. Harmonic has it backwards. The reason Harmonic was successful in challenging claim 9 is precisely the reason it lost on claim 11. For claim 9, Harmonic successfully argued that Haskell's encoder 100 disclosed both the claimed first switch and controller that regulated system data flow. Claim 11, however, contains an additional limitation requiring that the timing of video data switching from the first decompression array to the other decompression arrays be predefined *relative to the first switch and the controller*. Because Haskell's encoder 100 corresponds to both the "first switch" and "controller," the timing decisions made by Haskell's

system are not predefined relative to the first switch and controller as claim 11 requires.

For these reasons, the Board's judgment that claims 11-16 of the '291 patent are not unpatentable should be affirmed.

STANDARDS OF REVIEW

The Board's ruling that Harmonic's argument in reply was not responsive to Avid's Response and thus exceeded the permissible scope of reply is reviewed for an abuse of discretion. *Star Fruits S.N.C. v. United States*, 393 F.3d 1277, 1281 (Fed. Cir. 2005). The Board has been granted substantive rulemaking authority with regard to the "establishing and governing [of] inter partes review." *In re Cuozzo Speed Techs., LLC*, 778 F.3d 1271, 1279 (Fed. Cir. 2015) (citing 35 U.S.C. § 316(a)(4)). "It is well-established that deference is owed to decisions of the PTO in interpreting [its] regulations, . . . unless the interpretation is plainly erroneous or inconsistent with the regulation." *In re Lovin*, 652 F.3d 1349, 1353 (Fed. Cir. 2011).

The Board's ruling that Harmonic failed to present a sufficient case for the obviousness of claim 11 is a mixed question of law and fact. The ultimate determination of obviousness under § 103 is a question of law based on underlying factual findings. *In re Baxter Int'l, Inc.*, 678 F.3d 1357, 1361 (Fed. Cir. 2012) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966)). This Court

"review[s] the Board's factual findings for substantial evidence and review[s] its legal conclusions *de novo*." *Id*. Thus, the Board's finding that the Petition does not address the "predefined period of time" language of claim 11 is reviewed for substantial evidence. Likewise, the Board's finding that the Haskell "predefined system timing" feature was first disclosed in Harmonic's Reply is reviewed for substantial evidence. And what a reference teaches, and the differences between the claimed invention and the prior art, are questions of fact that are also reviewed for substantial evidence. *Id*.

ARGUMENT

I. The Board Did Not Abuse Its Discretion by Refusing to Consider an Improper New Argument Raised For the First Time in Harmonic's Reply

The Board correctly held that "Petitioner's arguments in the Reply are improper because they are not responsive to arguments raised in the Patent Owner Response. *See* 37 C.F.R. § 42.23." (A26.) The cited regulation states that "[a] reply may only respond to arguments raised in the corresponding opposition or patent owner response." 37 C.F.R. § 42.23(b). This rule has particular import in the case of the Petitioner's reply to the patent owner response because the patent owner has no opportunity to respond to any new evidence. Harmonic proffered the "predetermined system timing" feature of Haskell at this late stage. This new

evidence was highly prejudicial to Avid and was correctly disregarded by the Board.

A. Rule 42.23(b) Prevents the Fundamentally Unfair Practice of Improperly Springing Evidence on a Patent Owner at a Late Stage

The statutes and rules implementing IPRs are designed to force petitioners to lay out their case for unpatentability early in the proceeding—i.e., in the Petition itself. IPR petitions are subject to a number of particularity requirements. For example, "[a] petition . . . may be considered *only* if the petition identifies, in writing and *with particularity*, each claim challenged, the grounds on which the challenge to each claim is based *and the evidence that supports the grounds for the challenge*." 35 U.S.C. § 312(a)(3) (emphasis added).

Further, each petition must include "[a] *full* statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts." 37 C.F.R. § 42.22(a)(2) (emphasis added). The Federal Register provides the rationale for this rule:

> Sections 42.22(a)(1) and (a)(2) provide for a statement of precise relief requested, and statement of the reasons for relief. Vague arguments and generic citations to the record are fundamentally unfair to an opponent and do not provide sufficient notice to an opponent and creates inefficiencies for the Board.

77 Fed. Reg. 48,612, 48,620 (Aug. 14, 2012).

In an IPR proceeding, the patent owner has only two opportunities to defend against the attacks presented in the petition: (1) the preliminary response, which occurs before institution; and (2) the patent owner response, which is the patent owner's only opportunity to respond after institution. Harmonic's deficient Petition and late submission of evidence here denied Avid both of those opportunities to defend its property rights. Because Harmonic did not set forth its challenges in compliance with the applicable rules, Avid was prejudiced in its ability to defend its patent. Accordingly, the Board refused to consider the improper new argument, as it has done several times before. *See, e.g.*, *Scotts Company LLC v. Encap, LLC*, IPR2013-00110, Final Written Decision, Paper 79 at 5-6 (P.T.A.B. June 29, 2014) ("Specifically, we hold that the new evidence could have been included with the motion."); *BAE Sys. Info. and Elec. Sys. Integration, Inc. v. Cheetah Omni, LLC*, IPR2013-00175, Final Written Decision, Paper 45 at 15 (P.T.A.B. June 19, 2014) ("Although BAE cited Figure 20 in its Petition, it did not develop this particular argument in its Petition."); *Ariosa Diagnostics v. Verinata Health, Inc.*, IPR2013-00276, Final Written Decision, Paper 43 at 19 (P.T.A.B. Oct. 23, 2014) ("Petitioner… [fails to] explain[] why Exhibit 1010 could not have been presented as part of the asserted ground of unpatentability in the first instance with the petition."); *Toyota Motor Corp. v. Am. Vehicular Sciences LLC*, IPR2013-00424, Final Written Decision, Paper 50 at 21

(P.T.A.B. Jan. 12, 2015) ("Toyota cannot rely belatedly on this evidence in its Reply and Reply Declaration… to make up for the deficiencies in its Petition."); *Corning Inc. v. DSM IP Assets B.V.*, IPR2013-00047, Final Written Decision, Paper 84 at 14-17 (P.T.A.B. May 1, 2014).

In this regard, the Board's rules are no different than this Court's frequent and repeated admonishments that an argument made for the first time in a reply brief (whether in the agency below or in this Court) comes too late. *See, e.g.*, *Novosteel SA v. United States*, 284 F.3d 1261, 1274 (Fed. Cir. 2002) ("Raising the issue for the first time in a reply brief does not suffice; reply briefs *reply* to arguments made in the response brief—they do not provide the moving party with a new opportunity to present yet another issue for the court's consideration. Further, the non-moving party ordinarily has no right to respond to the reply brief, at least not until oral argument."); *see also Cross Med. Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1320 n.3 (Fed. Cir. 2005) ("new arguments raised for the first time in [a party's] reply brief" are waived).

B. Harmonic's Argument Regarding Haskell's "Predetermined System Timing" Feature Was New and Improper

Harmonic's treatment of claim 11 in its Petition was cursory (to put it generously). This was the entirety of Harmonic's argument with respect to this claim:

> **Claim 11**: Haskell discloses that the controller is capable of commanding the first switch to provide video data to the first video data decompression array at a first rate and to provide video data to the remaining video data decompression arrays at a second rate a predefined period of time after the first video data array begins receiving the video data at the first rate. For example, Haskell teaches the ability to individually control the incoming bitrate for each decoder. See Ex. 1008 at 2:28-32; 2:41-44. Haskell also discloses the ability to switch packets from disparate streams between a plurality of decoder units, one for each given stream. See, *e.g.*, demux switch 203 of Haskell (Ex. 1008) at Fig. 3, 13:35-54. Thus, all claim limitations are met. *See, e.g.*, Ex. 1002 ¶282.[5]

(A91.) This argument contained not a single word about Haskell's "predetermined system timing" feature. To the contrary:

- Column 2:28-32 discusses bit-rate selection, stating, "The actual transmission bit-rate selected may be chosen to be less than the maximum bit-rate allowed by the channel at a particular instant of time." (A289.)
- Column 2:41-44 also references bit-rate selection stating, "The encoder bit-rate for each encoder is controlled to prevent its associated encoder and decoder buffers from overflowing or underflowing." (*Id*.)
- Demux switch 203 is on the decoder side of the channel. Harmonic's position throughout the IPR is that "[e]ncoder 100 controls the flow of data through the decoder unit." (A89.)

[5] The Declaration simply parrots this paragraph, contributes no additional substance.

- Column 13:35-54 describes the function of demux switch 203 that works with switch controller 202 to identify the stream associated with a packet sent by encoder 100 and to route that packet accordingly. (A295.)

Neither in its Petition nor in the accompanying Declaration did Harmonic make a single reference to either "predetermined system timing" or Haskell 13:7-34, where that predetermined system timing is described. (A38-101; A102-77.)

Harmonic made its belated attempt to introduce Haskell's "predetermined system timing" feature in its Reply only after Avid pointed out in its Response that Harmonic had ignored this critical limitation in its Petition. Harmonic argued in its Reply—for the first time—that Haskell's "predetermined system of time" feature was relevant to claim 11:

> There is also no basis for Avid's contention that Haskell does not suggest "provid[ing] video data to the remaining video decompression arrays . . . a predefined period of time after the first video data array begins receiving the video data at the first rate." *Haskell explicitly discloses the use of predetermined system timing with regard to providing video data to decode buffers* (205-1, 205-2, 205-N). See Ex. 1008 at 13:7-54.

(A547 (emphasis added).)

Harmonic's strategic choice to introduce this new feature of Haskell in reply, by citing to and arguing from two new paragraphs of the Haskell reference that it had never before cited or discussed, is exactly the type of sandbagging behavior

that 37 C.F.R. § 42.23(b) was designed to protect against: a "reply may only respond to arguments raised in the corresponding opposition or patent owner response." The PTAB Trial Practice Guide further elaborates on this proscription, stating that "a reply that raises a new issue or belatedly presents evidence will not be considered. . . . Examples of indications that a new issue has been raised in a reply include [(i)] new evidence necessary to make out a *prima facie* case for the patentability or unpatentability of an original or proposed substitute claim, and [(ii)] new evidence that could have been presented in a prior filing." 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012); *see also* 77 Fed. Reg. 48,612, 48,620 (Aug. 14, 2012). Harmonic's belated argument fell squarely within both prohibitions. The new Haskell citation was apparently necessary for Harmonic to make out its *prima facie* case because Harmonic had submitted no evidence on that critical limitation in its Petition. And there is no legitimate reason why Harmonic could not have included this evidence in its Petition—Harmonic has offered none.

Harmonic's brief instead includes a litany of excuses as to why its late citation to Haskell's "predetermined system timing" feature was not really late, or in the alternative, was actually Avid's fault. Neither excuse holds up. For example, Harmonic protests that it did not have an opportunity to address the Board's refusal to consider its late citation. (HBr. 23-24.) This argument has a through-the-looking-glass quality, for it was *Harmonic* that chose to first cite to this new

evidence from Haskell in the *final brief* to be considered by the Board before its Final Written Decision.

Harmonic further argues that because Avid cited to a portion of the portion of Haskell that describes the "predetermined system timing" (*i.e.*, column 13:7-20) for an unrelated reason, that Harmonic was then free to allege for the first time that the "predetermined system timing" feature disclosed the critical (and missing) limitation of claim 11. (HBr. 24-26.) Avid's Response cites to that portion of Haskell—column 13, lines 7-20— one time on page 34 for the following proposition:

> The demultiplexer switch 203 has no control over when packets arrive, as that is encoder functionality in Haskell. (*Id*., 13:7-20.)

(A527.) This proposition has nothing to do with the "predetermined system timing" feature of Haskell, which is described in subsequent paragraphs that Harmonic never cited, discussed, or placed any reliance upon until its Reply. Further, the statement made by Avid is actually a statement with which Harmonic agrees. (*Compare* A89 ("[e]ncoder 100 controls the flow of data through the decoder unit") *with* HBr. 33 ("The PTAB, Harmonic, and Avid all agree that the encoder system of Haskell controls the bit-rate and timing through the system.").) In fact, Harmonic's entire case against the independent claims is built around Haskell's encoder 100 functionality being relevant to the claimed input switch and controller.

Because Harmonic actually agreed with Avid's statement, there was no reason or good cause for Harmonic to cite evidence at all.

Finally, Harmonic argues that because it disagreed with Avid's assertion that the cited portions of Haskell did not teach the critical limitation, Harmonic was free to submit new evidence in Reply. (HBr. 26-29.) This argument, were it to be accepted, would provide petitioners with a license to sandbag. Moreover, Harmonic's argument ignores 37 C.F.R. § 42.23(b), which limits replies to responding to arguments raised in the patent owner response. Avid's Response as to claim 11 shows how none of the four evidentiary citations to Haskell by Harmonic (*i.e.*, 2:28-32; 2:41-44; demux switch 203; and 13:35-54) relate to the critical limitation. (A527:4-A528:4.) Harmonic's Reply was thus properly limited to responding to that argument, not to scouring the Haskell reference to find some other, never-before-cited portion to prop up the deficiency in its case. Stated another way, Harmonic was free to argue that one or more of its four citations to Haskell did, in fact, teach the critical limitation. But Harmonic did not do that. Instead, Harmonic chose to cite a completely new, and previously unreferenced feature of Haskell as disclosing the critical limitation. This kind of tactic is often condemned in litigation as "sandbagging" or "laying behind the log"; whatever label might properly be attached to it, it was fundamentally unfair and violated 37 C.F.R. § 42.23(b) as well as the PTAB Trial Practice Guide.

In sum, Avid's Response with respect to claim 11 illustrated why each of Harmonic's four evidentiary citations to Haskell was wholly unrelated to the critical limitation of claim 11. In an attempt to plug this hole in its case, Harmonic then cited to the "predetermined system timing" feature of Haskell for the first time in its Reply, and argued that this never-before-cited, never-before-argued feature nonetheless satisfied that critical claim limitation. Because this new citation was not responsive to arguments raised in Avid's Response, and would have prejudiced Avid had it been allowed, Harmonic's late citation was properly disregarded by the Board.

II. Harmonic's Posturing Regarding the Board's Refusal to Consider Haskell's "Predetermined System Timing" Is Irrelevant Because the Board Actually Considered Harmonic's Argument

Harmonic's opening brief devotes more than nine pages as to why the Board's refusal to consider Haskell's "predetermined system timing" feature was a travesty of justice and an abuse of discretion. (HBr. 22-31.) But the brief fails to provide any discussion of why the predetermined system timing feature of Haskell matters. Harmonic's brief includes no explanation of how Haskell's predetermined system timing feature teaches the critical limitation. In fact, Harmonic's brief does not even bother to explain how the predetermined system timing feature of Haskell works. That feature is not even mentioned in Harmonic's technical description of Haskell. (HBr. 8-10.)

Thus, it appears that even Harmonic does not really believe that Haskell's predetermined system timing feature teaches the critical limitation. After 9-plus pages of lamentations about the Board's refusal to consider Harmonic's late-submitted evidence, Harmonic concludes its protest stating: "In sum, Harmonic's prima facie case . . . was sufficient to warrant a holding that claim 11 was obvious *regardless of whether* Haskell's 'predetermined system timing' teaches the predefined period of time' element of claim 11." (HBr. 31 (emphasis in original).)[6]

Harmonic's brief further fails to tackle the glaring fact that the Board actually did consider Harmonic's "predetermined system timing" feature argument and found it deficient. After not mentioning the "predetermined system timing"

[6] Harmonic likely distances itself from any explanation because a cursory understanding of the "predetermined system timing" feature of Haskell shows that it does not teach the critical limitation. Decoder switching of packets in Haskell is dependent on what packets are included in the periodically transmitted packs of packets and how those packets are encoded, decisions made by encoder 100. Packet switching by demux switch 203 is dependent on the origin of packets included in a pack of packets. If a pack includes five packets from stream "a" the switching will be different than if the pack includes a packet from stream "a," a packet from stream "b," a packet from stream "c," and a packet from stream "d." (*See, e.g.*, A295 at 14:12-31.) Because the encoder 100 is determining the identity of packets within a pack, the encoder 100 is determining the timing of demux switch 203's switching. Claim 11 requires that the transition from providing data from the first decompression array to the remaining decompression arrays be "predefined" relative to the controller/first switch. Because Haskell's "controller/first switch" is making the timing decisions, that timing is not in any way "predefined."

feature at all in the Petition, Harmonic included one relevant sentence in its Reply, asserting without explanation:

> Haskell explicitly discloses the use of predetermined system timing with regard to providing video data to decode buffers (205-1, 205-2, 205-N). *See* Ex. 1008 at 13:7-54.

After initially stating that it officially refused to consider this new evidence citation because it was untimely (A26 at ll. 9-22), the Board subsequently stated:

> In any event, even if Petitioner's arguments were to be considered, Petitioner does not explain sufficiently how Haskell's use of predetermined system timing for providing video data to decoder buffers (205-1, 205-2, 205-N), teaches or suggests a controller that commands the first switch to provide video data to the remaining video decompression arrays at a second rate a predefined period of time (*i.e.*, a prior defined period of time) after the first video data array begins receiving the video data at the first rate.

(A26 l.21-A27 l.4.)

Thus, in addition to finding Harmonic's late evidence procedurally improper, the Board also found it substantively lacking. To date, Harmonic has provided zero sentences in the Petition, one sentence in the Reply, and zero sentences in its opening appeal brief here explaining the import of the "predetermined system timing" feature of Haskell. The Board found that the one sentence provided was substantively unconvincing. In this appeal, Harmonic makes no attempt to address the fact that the Board did substantively rule on its procedurally improper "predetermined system timing" position. Indeed, despite the Board having noted the substantive deficiency of Harmonic's "predefined system timing" argument,

Harmonic still fails to explain the relevancy of Haskell's feature to the critical limitation of claim 11. Thus, the Board's Final Written Decision should be affirmed for the independent reason that it is correct on the merits.

III. Harmonic's Appeal Does Not Address, Let Alone Show The Presence, In Haskell, Of Providing Video Data To The Decompression Arrays At A Predefined Period of Time After The First Video Array Begins Receiving The Video Data

Avid and Harmonic appear to agree on most of the technical issues discussed by Harmonic related to claim 11. (HBr. 32-34.) But in addressing the merits of the Board's obviousness inquiry, Harmonic ignores Avid's argument in response that the Board found persuasive—that none of Harmonic's Petition citations to Haskell for claim 11 are related to the critical limitation where the controller commands the first switch to provide video data to the remaining decompression arrays *a predefined period of time after the first video data array begins receiving the video data*.

The Board, Avid, and Harmonic all agree that the encoder system 100 of Haskell controls the bit-rate and the timing through the Haskell system. (A460 (Institution Decision); HBr. 33.) Haskell discloses that the encoder may elect a bit-rate that is less than the maximum bit-rate allowed by the channel and that the bit-rate is controlled to prevent encoder and decoder buffer overflows and underflows. (A289 at 2:28-32; *id.* at 2:41-44.) As such, the amount of data received by each

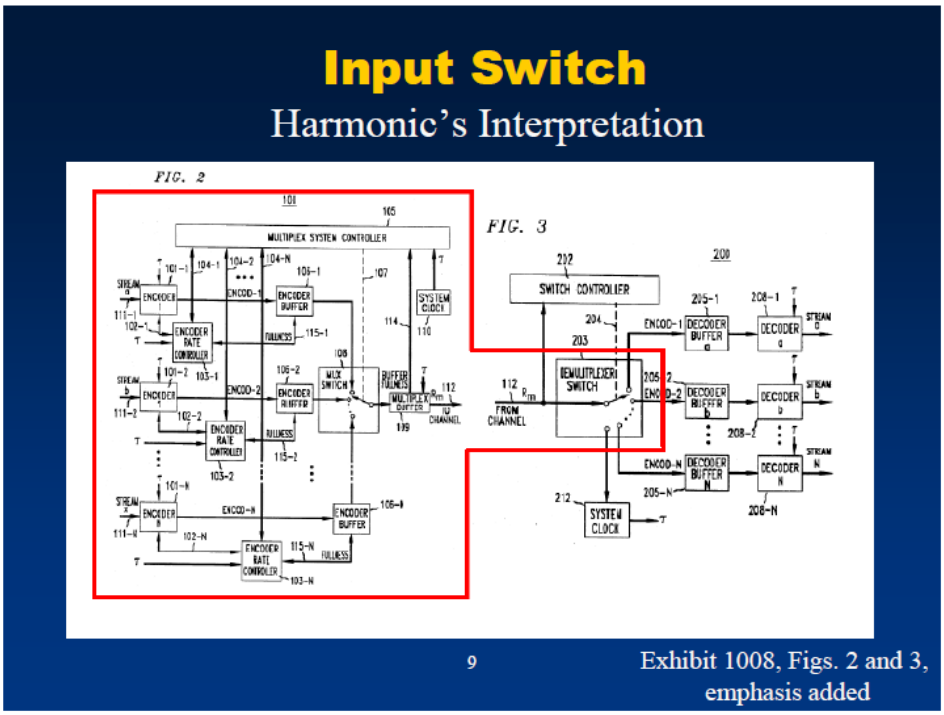
decoder and the timing by which that data is received is determined by the encoder 100.

Avid presented two arguments in its Response for claim 11. Harmonic focused only on the first, where Avid argued:

> First, the citations to column 2:28-32 and 2:41-44 describe encoder side functionality, where the encoder bit-rates are controlled to prevent buffer overflows and underflows. (*See e.g.*, Ex. 1002, 2:5-12; 14;12-14; 15:32-38; 16:7-9.) This disclosure regarding encoder side functionality is irrelevant to claim 11, which describes details of a video decompression controller.

(A526-527.) The Board disagreed with Avid's argument for independent claim 9 and dependent claim 11, finding that Haskell's encoder side functionality was relevant to the input switch and controller of Avid's claims. (A18-19.)

But Harmonic's victory on this point for claim 9 is precisely why Harmonic cannot prevail on claim 11. As Avid pointed out in its oral argument exhibits, Harmonic is pointing to Haskell encoder 100 as disclosing the claimed first switch and controller.



(A575, HBr. 16, 37.) Claim 11 requires that the timing of the switching of data from the first decompression array to the remaining decompression arrays be predefined relative to the controller. But Haskell's "first switch" and "controller" are the ones making the timing calls. Harmonic expressly admits that fact. (HBr. 33 ("The PTAB, Harmonic, and Avid all agree that the encoder system of Haskell controls the bit-rate and the timing through the system.").) Thus, the switching timing by Haskell's "first switch" and "controller" is not at all "predefined." Because the switching timing will change depending on the bit-rate selected by the encoder 100 (A289 at 2:5-13) and the identity and ordering of packets selected by the encoder 100 for transmitting (A295 at 14:12-31), Haskell fails to disclose the critical limitation where the controller commands the first switch to provide video

data to the remaining decompression arrays *a predefined period of time after the first video data array begins receiving the video data*.

Harmonic's arguments on appeal try to conflate the issues for claim 11. Harmonic argues that because Avid's first argument was not persuasive, Harmonic must win. As noted above, exactly the opposite is the case. Harmonic ignores Avid's second argument, which is the argument that the Board found convincing. Avid argued:

> Second, the citations to column 2 and the subsequent citation to the demultiplexer switch 203 of FIG. 3 at column 13 do not account for the "prede[fined] period of time" language of claim 11. The Haskell demultiplexer switch 203 connects the multiplex data stream 112 to the proper decoder buffer 205 as packets arrive. The demultiplexer switch 203 has no control over when packets arrive, as that is encoder functionality in Haskell. (*Id*., 13:7-20.) Thus, there is no "provid[ing] video data to the remaining video decompression arrays . . . *a predefined period of time* after the first video data array begins receiving the video data at the first rate," as required in claim 11.

(A527 (emphasis in original).)

This second argument explains why Harmonic's four citations to Haskell for claim 11 are not relevant to the critical limitation. The Board agreed:

> We agree with Patent Owner's argument that the Petition does not account for the "predefined period of time" language of claim 11 . . . .

(A26.) The Board additionally found that Harmonic's late evidence was also substantively deficient:

> In any event, even if Petitioner's arguments were to be considered, Petitioner does not explain sufficiently how Haskell's use of

> predetermined system timing for providing video data to decoder buffers (205-1, 205-2, 205-N), teaches or suggests a controller that commands the first switch to provide video data to the remaining video decompression arrays at a second rate a predefined period of time (*i.e.*, a prior defined period of time) after the first video data array begins receiving the video data at the first rate.

(A26-27.)

Harmonic does not contest Avid's arguments or the Board's finding that none of Harmonic's citations for claim 11 in the Petition or the Reply disclosed the critical limitation. Harmonic seeks now to sow confusion that Avid's lack of success on its first argument for claim 11 is determinative for claim 11. But Avid's second argument is the one that carried the day (A26-27), and Harmonic ignores it completely. Because Harmonic raises no questions regarding the actual reasons that the Board found claim 11 not unpatentable, that decision should be affirmed.

CONCLUSION

For the reasons set forth above, the Board's judgment that claims 11-16 of the '291 patent are not unpatentable should be affirmed. [7]

[7] We understand that the Solicitor's brief in this matter will separately address the propriety of the Board's so-called "redundancy practice." (HBr. 39-60.)

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on April 27, 2015, I caused the foregoing OPENING BRIEF OF PATENT OWNER-APPELLEE to be filed via CM/ECF with the Clerk of the Court, thereby electronically serving it on all counsel of record in this matter.

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CERTIFICATE OF COMPLIANCE

1. This brief complies with the type-volume limitation of Federal Rule of Appellate Procedure 32(a)(7)(B) because the brief contains 8,749 words, excluding the parts of the brief exempted by Federal Rule of Appellate Procedure 32(a)(7)(B)(iii) and Federal Circuit Rule 32(b).

2. This brief complies with the typeface requirements of Federal Rule of Appellate Procedure 32(a)(5) and the type style requirements of Federal Rule of Appellate Procedure 32(a)(6). The brief has been prepared in a proportionally spaced typeface using Microsoft Word 2007 in 14-point Times New Roman font.

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